CODIFICATION OF A FIELD PROGRAMMABLE ARRAY

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ABSTRACT

This project completed the design and codification of a Field-Programmable Gate Array (FPGA) to be used in the "Financial Monte Carlo Simulation on Architecturally Diverse Systems Project." [1] This simulation will be used to find the risk of a financial portfolio that has a probability of losing money on the market. The original project is divided into five stages; all of these stages have been simulated onto a multiple core computer and/or a graphics processor. Stages one and two were implemented using the Field-Programmable Gate Array (FPGA) code. For stage three of the project the Field-Programmable Gate Array (FPGA) was coded using a Hardware Description Language, the language selected to complete the project was Verilog. Stage three of this project consisted in adding a Field-Programmable Gate Array (FPGA) [2] integrated circuit. This implementation required a given equation which was used to code a matrix multiplication with a vector. This stage consisted of a square matrix and vector multiplication.

1. INTRODUCTION

Monte Carlo Simulation [3] is used in option pricing and risk management assessments. This simulation is needed to be in real time. To be able to accomplish this objective, a parallel processing implementation was necessary. Parallel processing, increases the number of computations per unit of time as oppose to a single processor implementation.

To accomplish this implementation, it was necessary to use a Field-Programmable Gate Array (FPGA) for certain portions of this project. This integrated circuit allows customizing the chip to have multiple components, which allows parallel processing. During stage three of the project, a Field-Programmable Gate Array (FPGA) was implemented and simulations were completed. The objective was to come up with a design and implement the design using a Hardware Description Language (HDL). The language of choice was Verilog.

2. RESULTS

In this project a Hardware Description Language was used to run simulations in a Field-Programmable Gate Array (FPGA). Verilog language was used to code the simulations in the FPGA. Before coding the simulations, several hardware designs were considered.

The stage three component designs consisted of one memory storage for the vector and a second storage residing outside of FPGA chip for the square matrix. The square matrix had to reside outside of the FPGA because the memory space needed was too large for the FPGA memory space available. Two numbers, 32-bits in size, were streamed into a six stage multiplier. After six clock cycles the result of the first number showed. The six stage pipeline was chosen because this was the optimum performance according to the Xilinx Core Gen software. After the multiplication, the

resulting 64-bits were input into an accumulator which accumulated the numbers coming in until the reset was used. Another design that was considered replaced the single port RAM with a dual FIFO system with feedback on each FIFO. The objective was to keep a continuous stream of data coming in while doing the computations. The first FIFO was first filled with the data, and after its completion the second FIFO began filling up with the second vector and while the second vector was filling up the first vector started the multiplication process with the matrix. The feedback was used to reuse the data necessary to do the matrix and vector multiplication.

3. CONCLUSION

At the conclusion this eight-week project, the multiplier and accumulator had been debugged and simulated, but the dual FIFO system needed to be simulated. Both of these parts need to be implemented onto an actual Field-Programmable Gate Array (FPGA) to test whether or not the FPGA's behavior is exactly the same as that produced during the simulation.

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